## ONLINE COMPUTING DICTIONARY



# VHDL

Very High Speed Integrated Circuit (VHSIC) Hardware Description Language. A large high-level VLSI design language with Ada-like syntax. The DoD standard for hardware description, now standardised as IEEE 1076.

["VHSIC Hardware Description Language", M.R. Shahdad et al, IEEE Computer 18(2):94-103 (Feb 1985)].

**Previous**: Very Small Aperture Terminal, VESA, VESA Local Bus, V.FAST, VFAT, V.FC, vg, VGA, VGQF, vgrep, VGX

**Next**: VHE, VHLL, vhost, VHS, vi, Vic20, video adapter, video card

# EE497i - Rapid System Prototyping

## XILINX M1-TOOL Quick-Start Tutorial

### Preliminary Steps to do before you invoke the M1 tools for the first time:

**Step a:** Copy the .xnf files present in the system that you need incase your design generates latches when you use Synplicity. Go to the directory where synplicity has created the XNF file of your design. Then use the following command.

**cp /opt6/synplcty/lib/xilinx/*.xnf .**

This will copy all the .xnf files that the M1 tools need in case your synthsis run generates latches

**Step b:** Copy the lines below into a file with the same name as your design name but with extention .ucf (e.g. hw4.ucf) and save it in the directory where you have placed the XNF file (e.g. hw4.xnf) produced by Synplicity synthesis. This is your USER CONSTRAINTS FILE which assigns outputs to the bar-graph LEDs and inputs to the DIP switches. Note the signal naming convention, and make any necessary changes so that the NET names correspond exactly to those of your design.

```
NET "clk" LOC = "p13";
NET "h" LOC = "p23";
NET "l" LOC = "p19";
NET "r" LOC = "p20";
NET "la" LOC = "p65";
NET "lb" LOC = "p62";
NET "lc" LOC = "p61";
NET "ra" LOC = "p58";
NET "rb" LOC = "p59";
NET "rc" LOC = "p60";
```

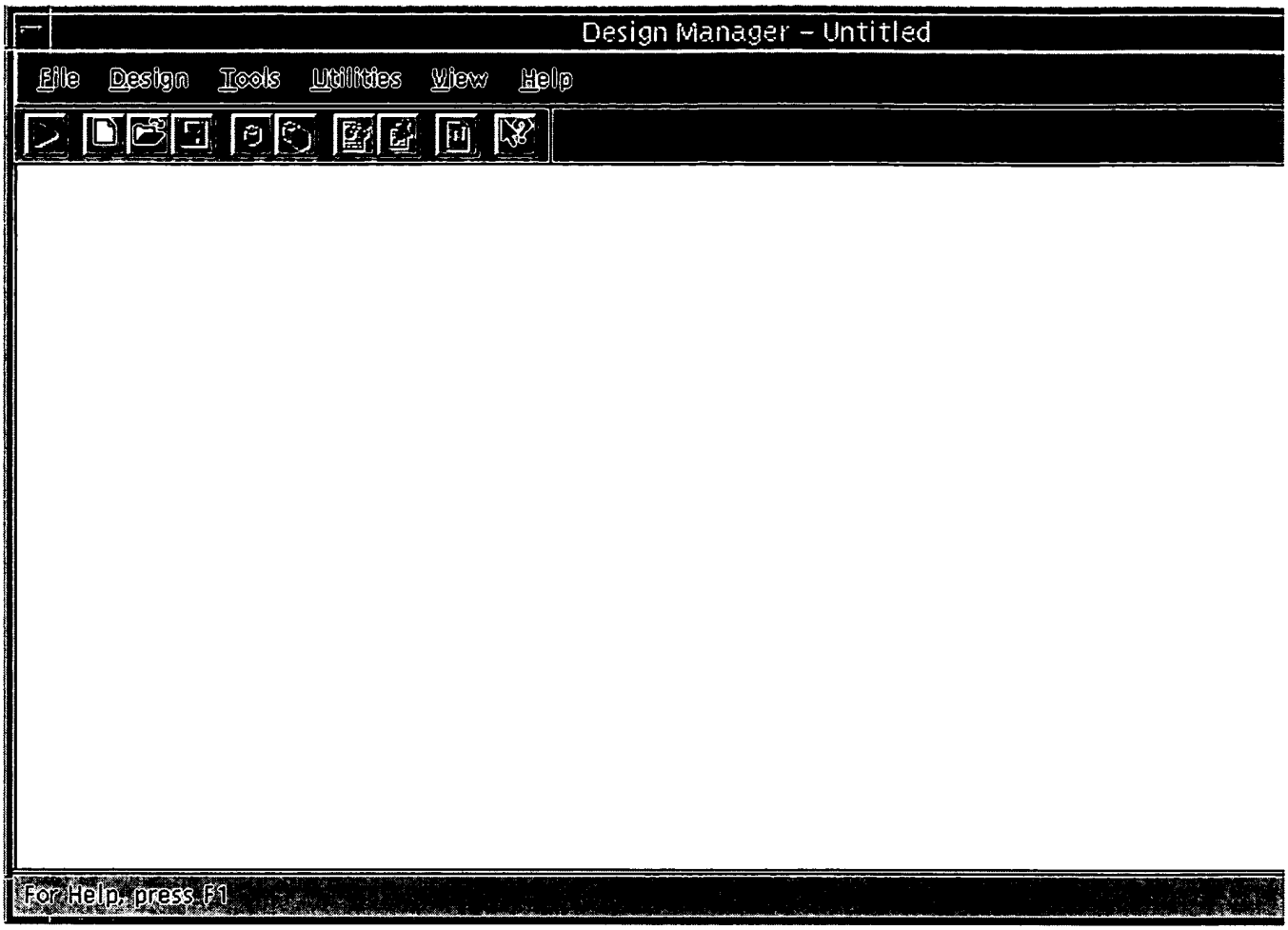
Note : You can also edit this constraints file from the M1 tools under the Design Manager under the Utilities Option. (clk, h, l, r , ra, rb, rc, la, lb, lc) are the ports of entity. You can change them to what ever names you have chosen in your entity description.

**Step c :** Use the xildoc & command and go into Hardware and Peripherals User guide; then go into the Table of Contents to look into the details of the demo board. Here you can find what the above pins (the ones mentioned in constraints file) are. They are input and output ports connected to DIP switches and LEDs. Note that pin 13 is used exclusively for clock (the 20 Mhz oscillator clock located on the Demo Board). You can also use extra pins in case you need them for debugging, and accordingly include them in your .ucf file which is the constraints file.

### To use M1 tools follow these sequence of steps:

**Step1 :**

**Type xactm1 & at the unix prompt. Design Manager will open and looks like the the screen below**



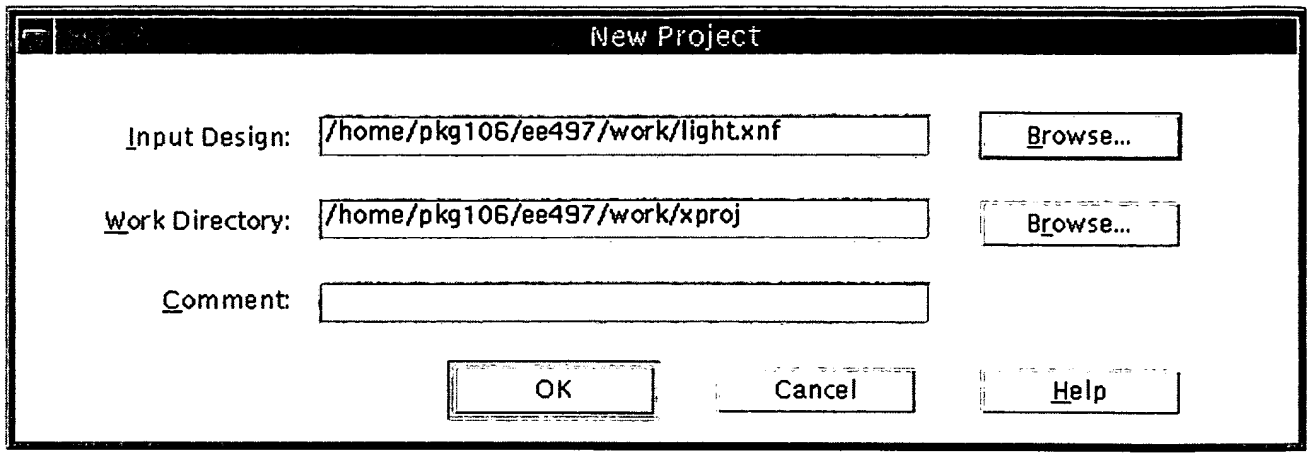

**The Tools Menu has sub-options: FLOW ENGINE, TIMING ANALYZER, FLOOR PLANNER, PROM FILE FORMATTER, HARDWARE DEBUGGER, EPIC DESIGN EDITOR and these are the tools that Design Manager invokes when you click appropriate icons/commands.**

**The Design Menu has sub-options like IMPLEMENT ... FPGA Multi - Pass Place and Route etc.,**

**There are some icons on the right. They aren't activated now because a project hasn't been selected. Once you open a new project they become activated and use can use them.**

**Step2 :**

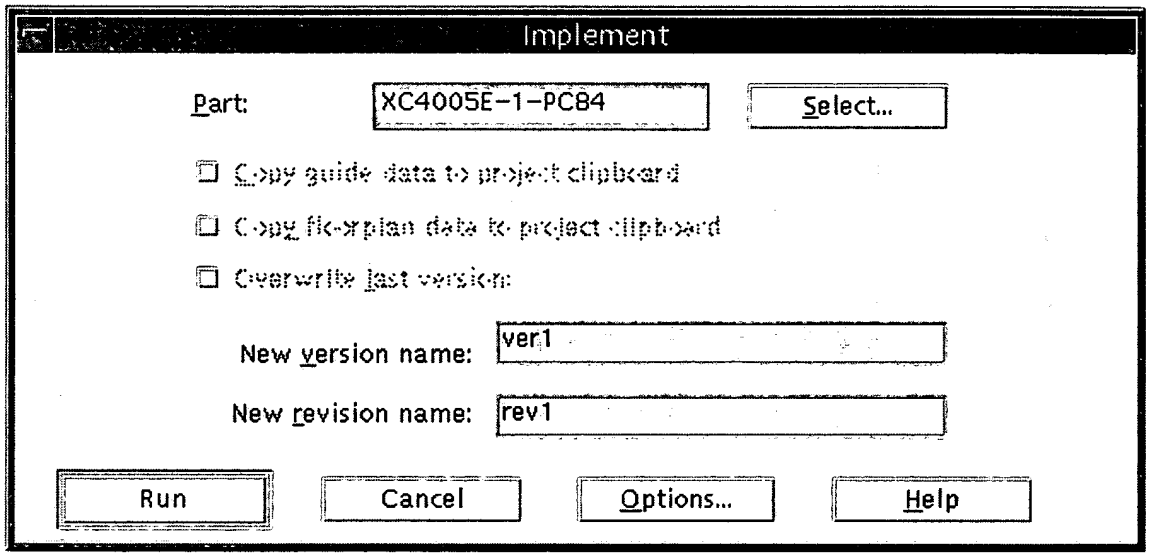
**Click File menu and click New Project ...option to create a new project. A New Project form pops up .**




**Use the Browse option to input the design, which is the .xnf file that Synplicity has generated. Click Ok after you are done. This will get you back to the Design Manager**

**Step 3:**

**In the Design Manager, Click Design Menu and click the Implement option and the following window pops up.**




**ver1 and rev1 are the directories that are created under the project directory xproj. It is in these directories that all the files that various tools generate are stored.**

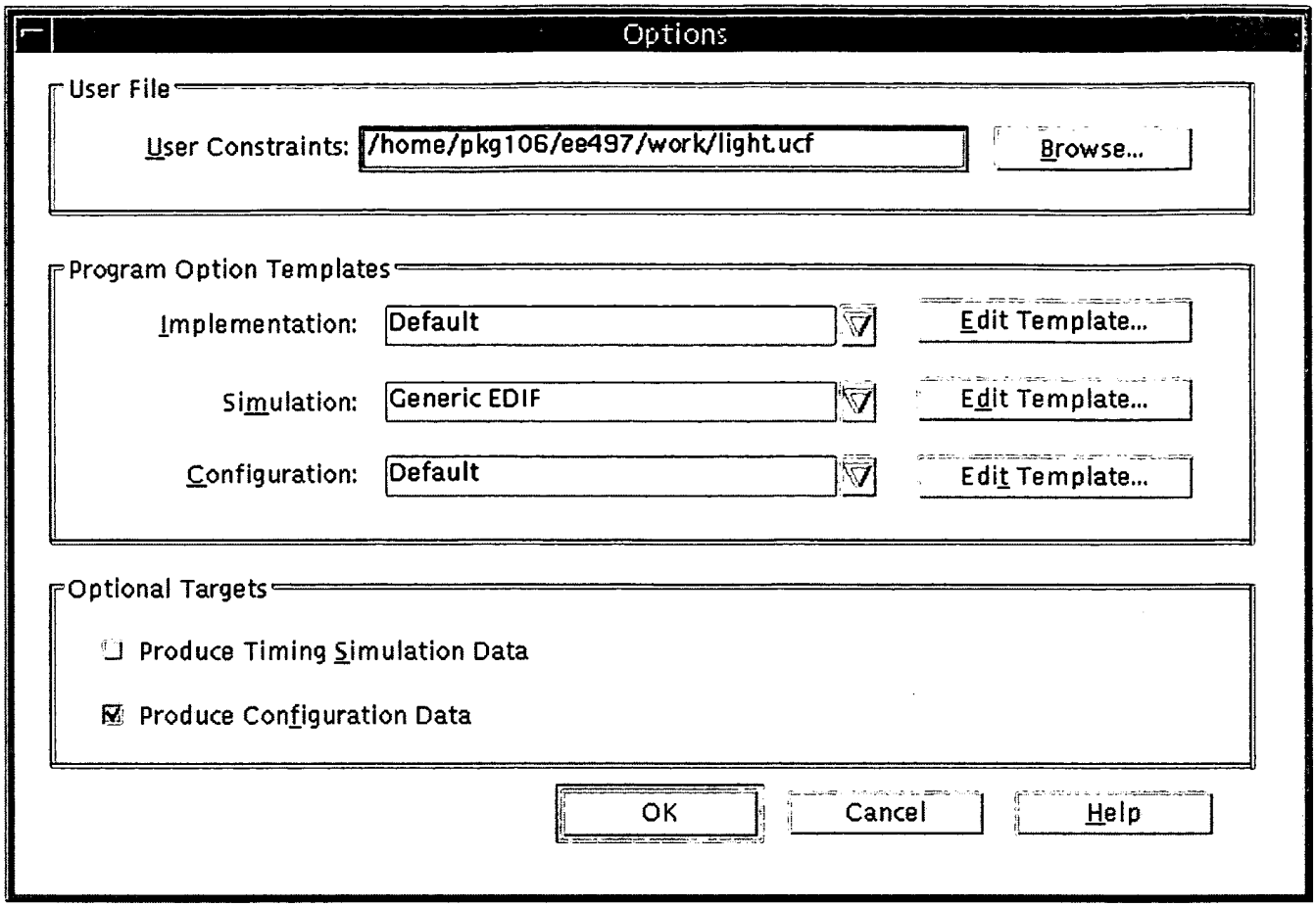
**Note : You can see the other options lke Overwrite Last version etc., which are not activated right now. You can use that option when you are running the tools the next time inorder to avoid multiple copies(that are stored as rev1, rev2, rev2. etc) of your designs.**

**Select XC4005E-1-PC84 as the part from the select ... option**

**Step 4:**

**Click Options... tool bar at the bottom to include the constraints file. The following window pops**

**up.**

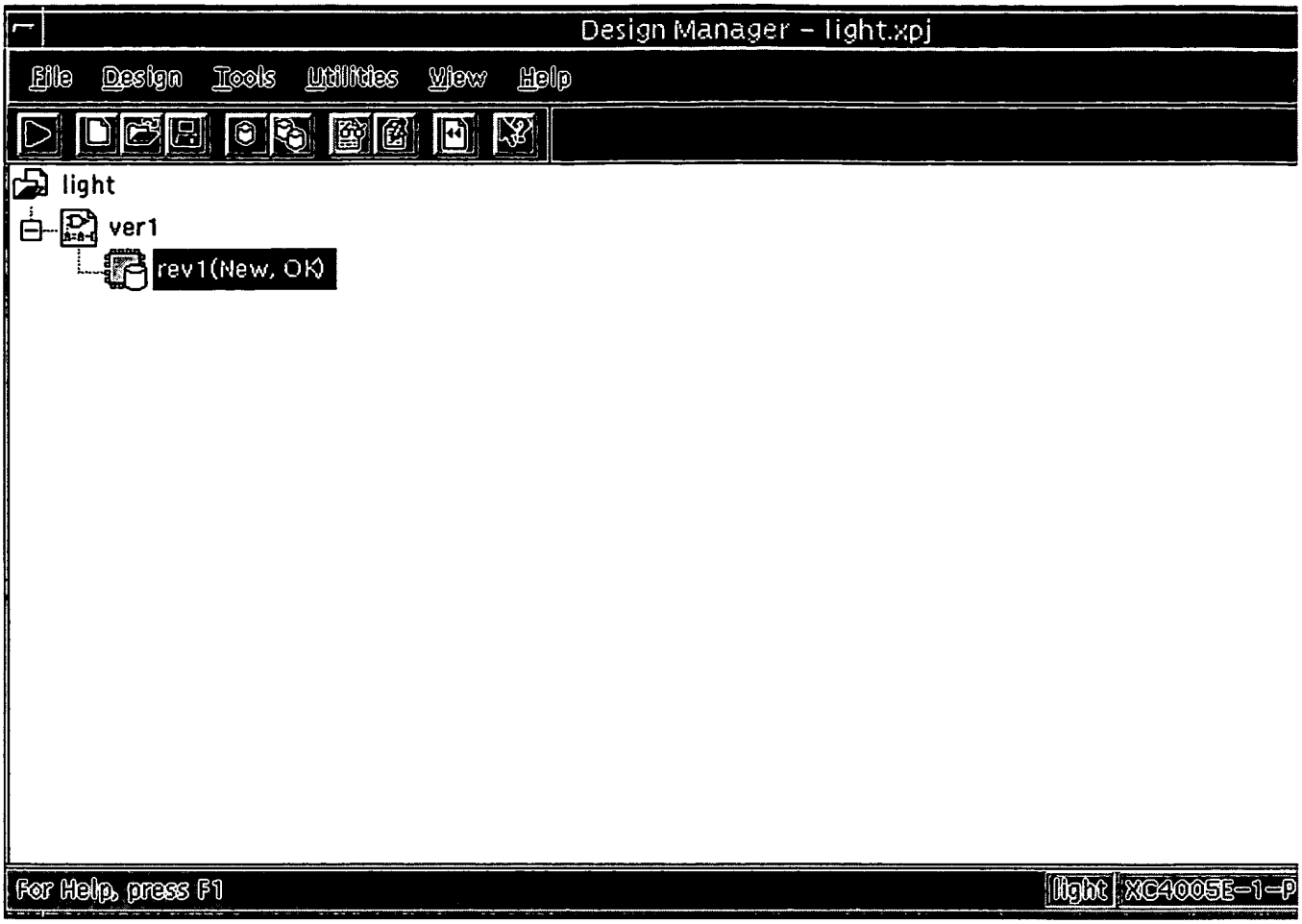



**Include the constraints file(.ucf) by locating it using the Browse option. Then click ok. This will get you back to the Implement window**

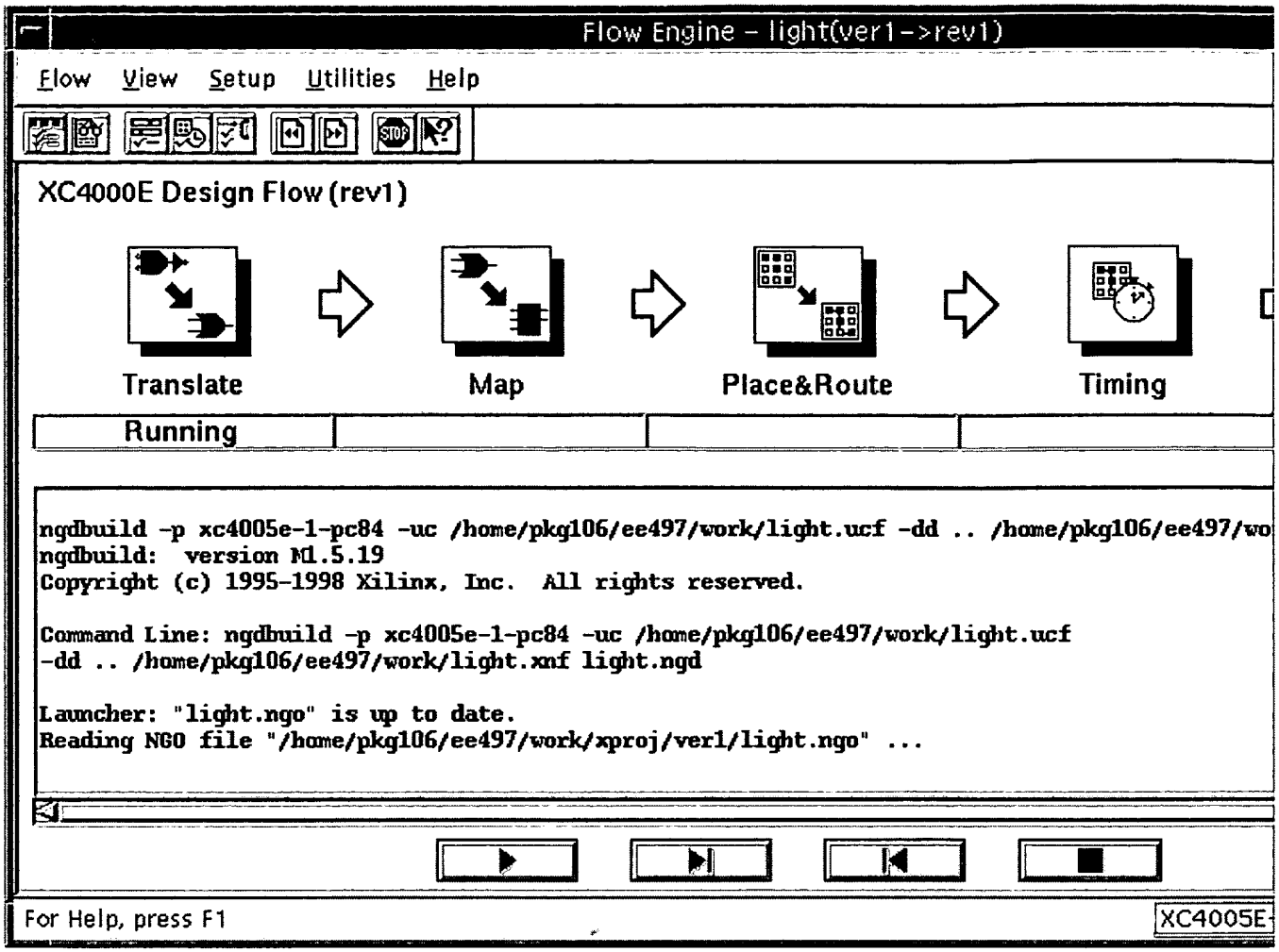
**Step 5:**

**Click Run in the Implement Window**

**This will use the constraints specified in the constraints file and Design Manager now looks like this. This shows that the hierarchy structure that is created inorder to store the various files that the tools generate. Now you can notice the icons on the right are activated meaning they can be used now.**




**Simultaneously, the Flow Engine starts implementing and the following Flow Engine window also pops up.**

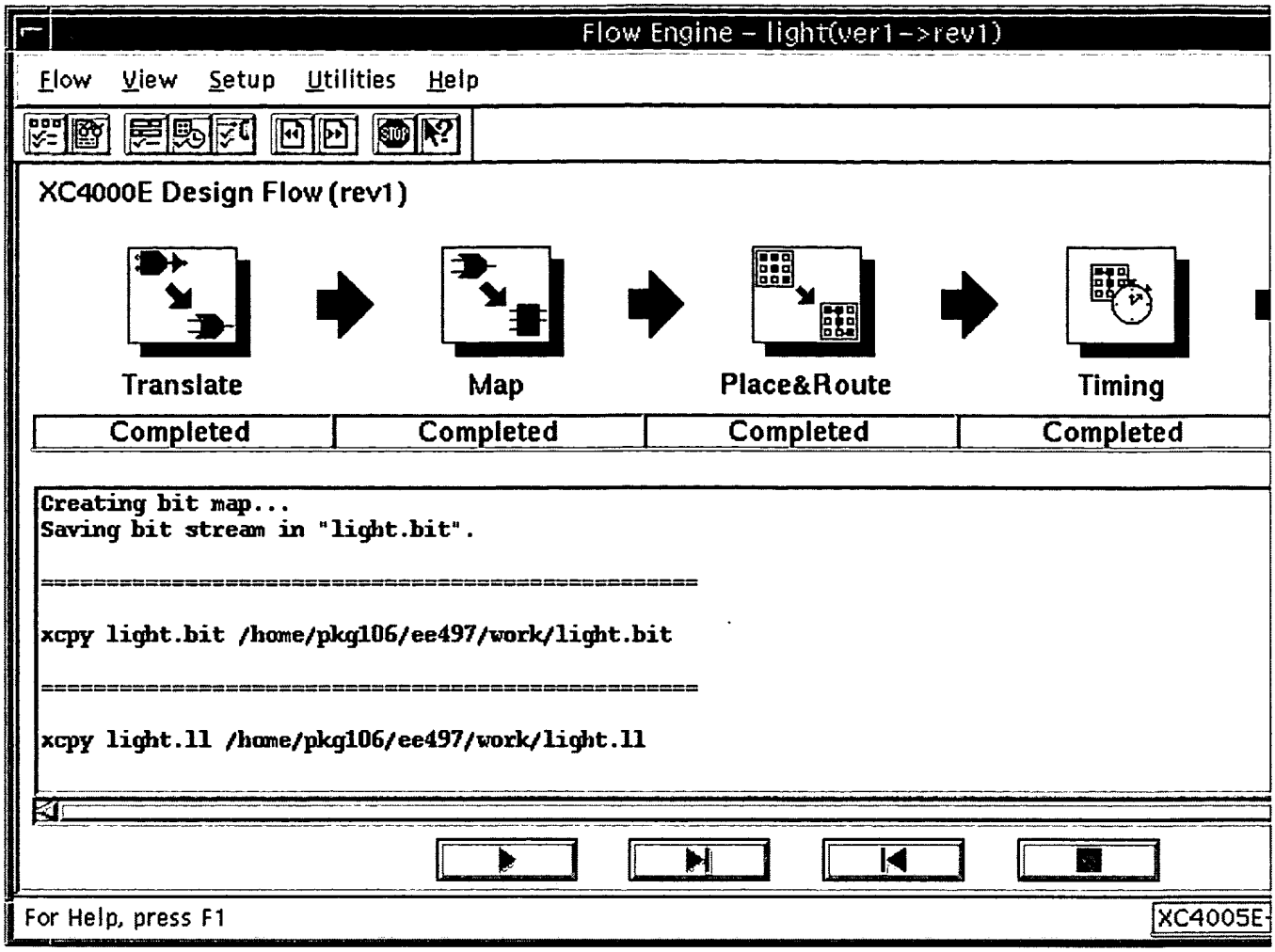



**You can see the various steps in the implementation process like Translate, Map, Place & Route, Timing, Configure running one after the other. You can see the status of each step whether it is running or completed or aborted. You can use the icons at the bottom(left to right) to continue till the end, move forward one step , move backward one step, to stop immediately.**

**Note : You can use the Stop sign( one of the icons in the top) to specify after which step you want to stop the process. By default it will stop after after finishing configuration step**

**Step 6.**

**Once the implementation process is finished you will see the Flow Engine to look like this indicating that it has finished Translating, Mapping, Place & Route, Timing Analysis and Generating Bit file (Configure).**




**You can also step back and restart the implementation process by using the icons at the bottom as explained in the above step.**

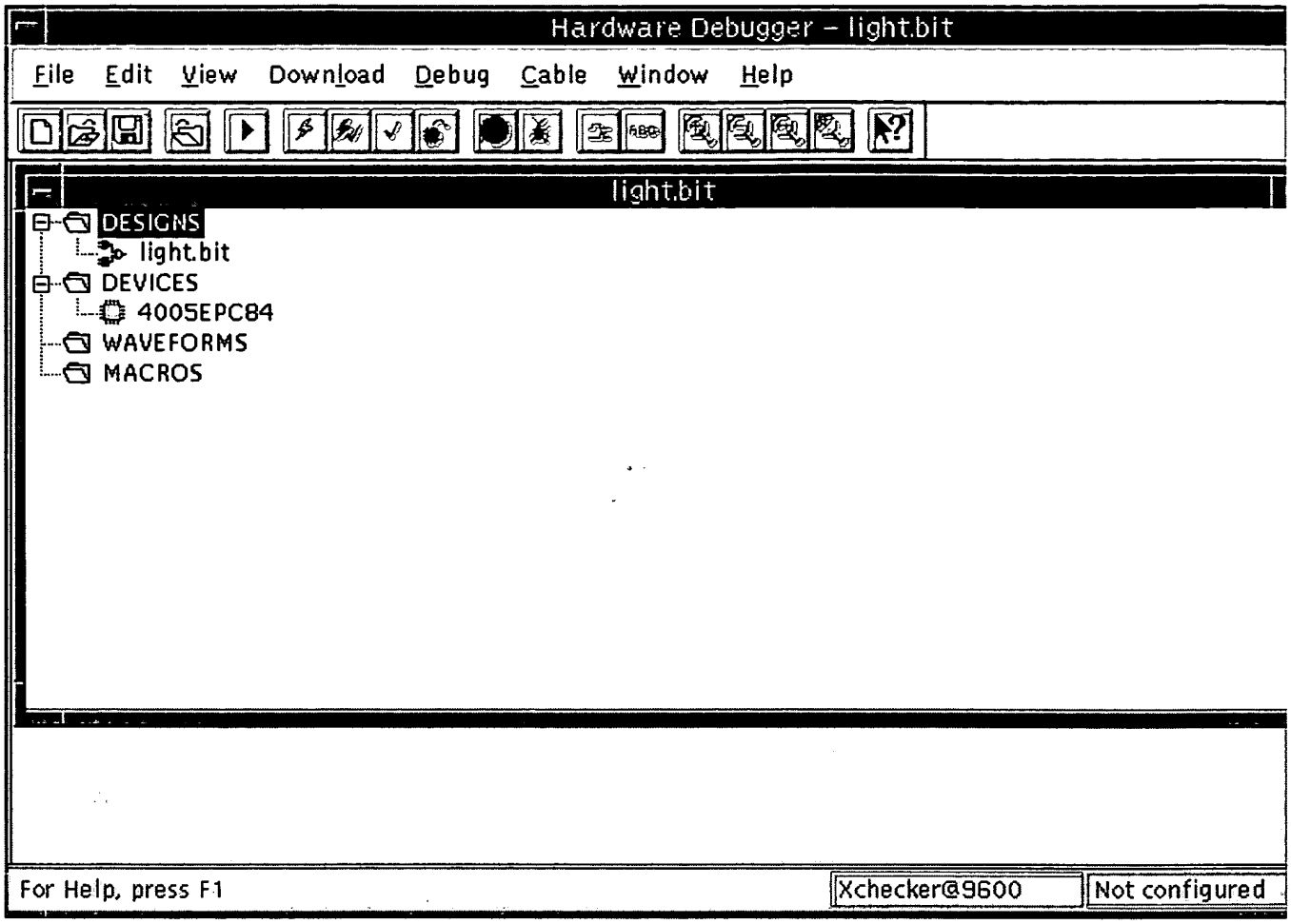
**Step 7 :**

**Ensure that the XChecker cable is connected to the SERIAL A ( or SERIAL B) port on the back of the SPARC5, that the cable head is connected to the DEMO BOARD, and that power in ON to the DEMO BOARD( Switch 1 on DIP SWITCH SW 2 - labeled power - is ON and the decimal points are lit up on the left two 7-segment displays).**

**Step 8 :**

**Get back to the Design manager to invoke the Hardware Debugger to download the bit file onto the FPGA.**

**Click Hardware Debugger in the Tools menu and the following window pops up**

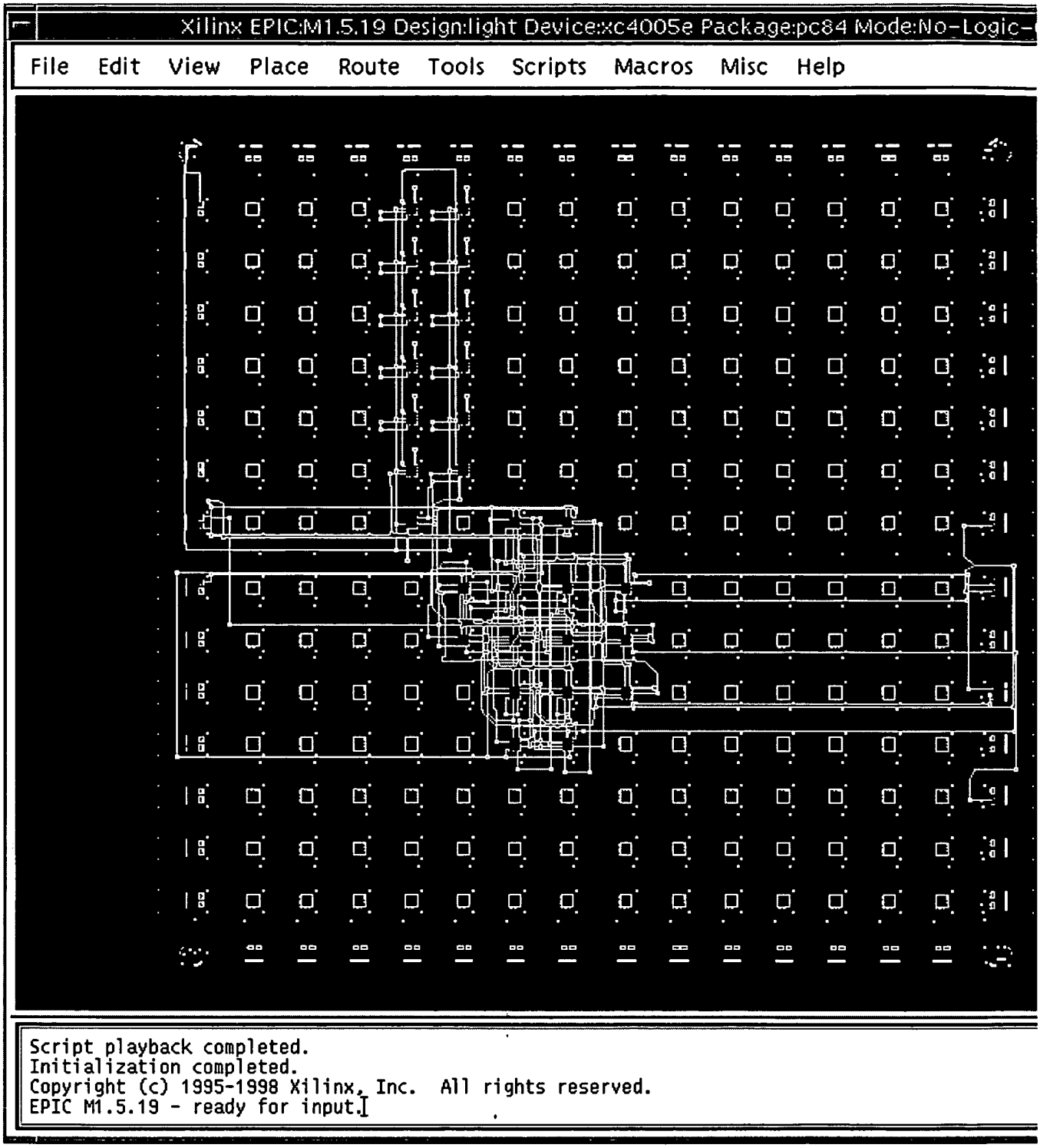



**Step 9 :**

**Click the Download Design option in the Download Menu to start downloading the bit file onto the FPGA. Once the downloading is finished, you can test your design by using the DIP switches that you used to specify the inputs.**

**Step 10 : (Optional but Highly Recommended)**

**You can view the details of your "placed and routed" design in terms of how the CLBs and IOBs are used. Click the Epic Design Editor option under the Tools menu in the Design Manager.** Explore the EPIC menu options to see what physical design information is available.


Xilinx EPIC:M1.5.19 Design:light Device:xc4005e Package:pc84 Mode:No-Logic-
File Edit View Place Route Tools Scripts Macros Misc Help
Script playback completed.
Initialization completed.
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EPIC M1.5.19 - ready for input.